FORM PTO-1390 (REV. 1-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

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U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	
09/341633	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP98/00233	January 22, 1998	January 23, 1997

TITLE OF INVENTION

PROGRAMMABLE DISPLAY DEVICE

516 Rec'd PCT/PTO 15 JUL 1999

APPLICANT(S) FOR DO/EO/US

NAKAMURA, Satoshi; YAMAMURA, Hiroyuki; YAMAMOTO, Shinzi and MORIYA, Masaaki

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(3)).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(2)).
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☒ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98./International Search Report

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
    1.) Letter of Corrected Formal Drawings with two (2) sheet(s) of formal drawings

    2.) Twenty-one (21) Sheet(s) of Formal drawings

U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	INTERNATIONAL FILING DATE	ATTORNEY'S DOCKET NUMBER
09/341633	PCT/JP98/00233	80 Rec'd PCT/PTO 15 JUL 1999	1152-237P

17. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(5):		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$970.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$840.00**		
International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO. **$760.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$670.00**		
International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4). **$96.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 840.00	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$ ---	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	9 - 20 =	0	X **$18.00**	$ ---	
Independent Claims	1 - 3 =	0	X **$78.00**	$ ---	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		none	+ **$260.00**	$ ---	
			TOTAL OF ABOVE CALCULATIONS =	$ 840.00	
Reduction of ½ for filing by small entity, if applicable. Verified Small Entity statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28).				$ ---	
			SUBTOTAL =	$ 840.00	
Processing fee of **$130.00** for furnishing the English translation later than ☐20 ☐30 months from the earliest claimed priority date (37 CFR 1.492(f)).			+	$ ---	
			TOTAL NATIONAL FEE =	$ 840.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). **$40.00** per property			+	$ 40.00	
			TOTAL FEES ENCLOSED =	$ 880.00	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of $ **880.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account. No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 02-2448.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

Send all correspondence to:
Birch, Stewart, Kolasch & Birch, LLP
P.O. Box 747
Falls Church, VA 22040-0747
(703)205-8000

SIGNATURE

GORENSTEIN, CHARLES
NAME

29,271
REGISTRATION NUMBER

/mp July 15, 1999

1152-237P

IN THE U.S. PATENT AND TRADEMARK OFFICE

APPLICANT: Satoshi NAKAMURA et al.

INT'L. APPLN. NO.: PCT/JP98/00233

SERIAL NO.: New GROUP:

FILED: July 15, 1999 EXAMINER:

FOR: PROGRAMMABLE DISPLAY DEVICE

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents July 15, 1999
and Trademarks
BOX PATENT APPLICATION
Washington, D.C. 20231

Sir:

The following Preliminary Amendments and Remarks are respectfully submitted in connection with the above-identified application.

IN THE SPECIFICATION:

Before line 1, insert --This application is the national phase under 35 U.S.C. §371 of PCT International Application No. PCT/JP98/00233 which has an International filing date of January 22, 1998 which designated the United States of America.--

R E M A R K S

The specification has been amended to provide a cross-reference to the previously filed International Application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By

CHARLES GORENSTEIN
Reg. No. 29,271
P.O. Box 747
Falls Church, VA 22040-0747

(703) 205-8000
CG/tnp

(Rev. 2/19/99)

DESCRIPTION

PROGRAMMABLE DISPLAY DEVICE

Technical Field

The present invention relates to a programmable display device in a computer system which displays image data, in particular, to a system which reads data for the display from a memory in a graphic display system very flexibly, and can define dynamically the minimum unit of the pixel data to be read out for every pixel, when reading the data for the display from the memory.

Background of Art

Conventionally, in a standard computer, the superposing and synthesizing processing of the display data in a single frame memory is performed directly by a main processor or portrayal device on the memory. FIG. 1 is a block diagram showing one embodiment of the conventional image display device. This image display device is composed of a main CPU 101, a main memory 102, a data processing circuit 103, a line memory 104, an output processing circuit 105, a system controller 106, and a sync signal generating circuit 107.

In the main memory 102, some display data are stored. For example, considering a case where several kinds of window display are performed, display data corresponding to each

window is stored. When these windows are superposed and displayed on one screen, the main CPU 101 selects and reads each display data so as to obtain one screen-display, and stores again the display data for one screen in the main memory 102. The system controller 106 generates an address of the main memory 102 for the data transfer, according to the timing of the sync signal generated by the sync signal generating circuit 107. After the display data is read out from the main memory 102 according to this address, and a predetermined data processing is performed by the data processing circuit 103, the data is transferred to the line memory 104. The data from the line memory 104 is output according to the timing of the sync signal, subjected to the processing for display by means of the output processing circuit 105 and displayed on the display.

Furthermore, as disclosed in Japanese Patent Application Laid-Open Hei 6 No. 149527, there is a system in which frame memories are prepared for the numbers necessary for superposition, the data is read out from all the frame memories at the time of outputting the picture, and the synthesized results are displayed based on the priority among respective frames.

Moreover, as disclosed in Japanese Patent Application Laid-Open Hei 6 No. 295169, there is a system which identifies which mode (for example, the bit number of one pixel) each

display dot is in by providing an identification memory for every display dot of the memory in the display area separately from the memory for display, and displays the display dot according to the mode, and displays a different display mode on one screen.

In addition, there is a system which references the content of the identification memory, or a system which utilizes a separate mask memory and when the information in each window now being displayed is changed and rewritten, masks the outside of the area, as disclosed in Japanese Patent Application Laid-Open Hei 7 No. 334342.

When the main CPU 101 performs the processing such as superposition and the like of each window, however, the burden of the main CPU 101 becomes too much, resulting in such a problem that the main CPU 101 cannot perform other processing to decrease the overall processing speed.

Furthermore, in a method to reduce the processing load of the software by having frame memories for the numbers required to superpose each window, it is required from the initial stage to have the frame memories of the maximum numbers to be considered necessary. Namely, regardless of the size of the window to be displayed on the screen, the frame memories are required in the maximum size of the display area. Therefore, the efficiency of using the memory is decreased, and when a number of windows are open at the same time, it

is required to read out the data simultaneously from the whole frame memories corresponding to the window. Namely, it is necessary to read out the data whose window is superposed and not displayed actually. Thus, the consumed power becomes large proportional to the number of windows opened on the screen.

Furthermore, as a method to mingle and display different display modes on one screen as in the conventional device, there can be mentioned a method to identify which mode each display dot is in by providing identification memories for each display dot of the memory in the display area. In this method, since the identification memory of several bits becomes necessary separately for the memory for the full screen, a memory (identification memory) becomes necessary on the side which cannot be used for other applications. Similar thing can be said when the mask memory is used.

It is an object of the present invention to provide a programmable display device which requires only a memory space for storing the display data, and which can increase the processing speed by reducing the number of access to the memory for the display and reduce the burden of the main control section.

Disclosure of the Invention

The present invention has been developed in order to

attain the above object, and the aspect thereof is as follows.

The first aspect is a programmable display device comprising:

a main memory which stores the display data;

a data processing circuit which converts the data format of said display data into the data format of the screen display;

a number of line memories which store the display data converted by said data processing circuit per unit of the display line;

a display control section which controls the transfer and storage of the display data from said main memory to/in said line memory and the readout of the necessary display data from said line memory to display it on the screen; and

a main control section which controls the storage of said display data in said main memory, and the transfer of the stored information including the data format and the storage address to said display control section, wherein

said display control section reading out said display data by specifying the address of the display data for one line which has a possibility to be displayed on the screen to said main memory from which the display data is transferred, based on said stored information, causing said data processing circuit to perform the data transfer and select said line memory to store said display data.

The second aspect of the present invention is a programmable display device according to claim 1, wherein said display control section controls the storage of the display data to be utilized repeatedly in said line memory, so that when the repeated display data is displayed, said repeated display data is read out from said line memory by specifying the address thereof and displayed on the screen.

The third aspect of the present invention is a programmable display device according to claim 1, further comprising a data buffer memory for storing the display data to be utilized repeatedly, and when said data is displayed on the screen, said display control section causes said repeated display data to be read out from said data buffer memory and displayed on the screen.

The fourth aspect of the present invention is a programmable display device according to claim 1, which includes:

a first buffer memory for storing the display data read out from said main memory;

a second buffer memory for storing the display data read out from said first buffer memory; and

an address counter for counting the readout address and the write address of said first and the second buffer memories; wherein

said display control section controlling the stop and

motion of the readout address count and the write address count, respectively, with respect to said address counter, performing the processing of expansion, contraction and skip and storing the data in said line memory.

The fifth aspect of the present invention is a programmable display device according to claim 4, wherein said display control section causes the stop and motion of the readout address count to be repeated in a predetermined order.

The sixth aspect of the present invention is a programmable display device according to claim 1, wherein said data processing circuit has a plurality of conversion processing circuits for converting various data formats, and said display control section selects said conversion processing circuits based on the data format information of said stored information.

The seventh aspect of the present invention is a programmable display device according to claim 1, wherein said display control section is provided with a program memory and a data memory for storing the necessary programs and data.

The eighth aspect of the present invention is a programmable display device according to claim 7, wherein said display control section causes the information necessary for said program memory and said data memory to be transferred from said main memory.

The ninth aspect of the present invention is a programmable display device according to claim 1, wherein said display control section adds the line information showing in which line the data is to be used when storing the display data in said line memory, and controls the display of the data in such a manner that when reading out the display data from said line memory, the line information is read out simultaneously and the data is displayed only when the line which uses said display data is the same with the line information.

In the invention of said aspect 1, the display data of the portion required at the time of display is taken out from the main memory and used. Therefore, it is possible to take out the data at an optional position in the main memory and combine them optionally. This control is performed by the display control section, thus the main control section need not perform the processing, hence the processing load of the main control section in the software can be reduced.

In the invention of said aspect 2, when the data is to be repeated in the line direction, as the background in the window system, the readout line memory address can be looped in an optional position.

In the invention of said aspect 3, since the cursor and the repeated background can be stored in the data buffer memory, it is not necessary to read out the routine data from

the main memory. Thus, the number of use of the data bus can be reduced.

In the invention of said aspect 4, it is not necessary to perform the expansion/contraction processing with respect to the data for the display in advance, in order to perform the expansion/contraction processing when the display data is read out, hence the efficiency of using the bus can be increased. In addition, when the video input picture is displayed, it is normal that the change of the picture size is required, but by performing the expansion/contraction processing at the output stage, the expansion/contraction circuit can be utilized more effectively. Thereby, while taking in the video data always in a full size, the display can be set in an optional size without the need of transferring the data to the frame memory or the like.

In the invention of said aspect 5, expansion and contraction at a certain magnification can be performed with a simple processing, by repeating the stop/motion of the readout address count from the first buffer memory in a predetermined order.

In the invention of said aspect 6, since the display control section can perform the data conversion based on the data format information in the stored information, the format to store the data for the display is not particularly limited.

In the invention of said aspect 7, since there are

provided a program memory and a data memory for storing the program and the data necessary for said display control section, it is not necessary to read out the data from the main memory every time of processing.

In the invention of said aspect 8, said display control section can flexibly correspond to the change of the screen mode or the graphic area so as to transfer the information necessary for said program memory and said data memory from the main memory. Since the program or the data exceeding the capacity can be read out from the main memory, the capacity of the memory may be small.

In the invention of said aspect 9, it is not required to delete the data in the line memory every time each line is displayed, and the used line information in the line memory has only to be deleted for every period of vertical retrace, hence the processing can be performed at a high speed.

Brief Description of the Drawings

FIG. 1 is a block diagram showing one embodiment of the conventional image display device.

FIG. 2 is a block diagram showing one embodiment of the image display device according to the present invention.

FIG. 3 is a block diagram showing the data processing circuit and the display memory section of this image display device.

FIG. 4 is a block diagram showing the display processor of this image display device.

FIG. 5A ~ FIG. 5C are diagrams illustrating the display data of the main memory and the display output of the display.

FIG. 6 is a flow chart for displaying beta screen data for one screen.

FIG. 7 is an example of the display screen of the beta screen.

FIG. 8 is a memory map of the main memory in which the beta screen data is stored.

FIG. 9 is a memory map of the main memory in which various display data are stored.

FIG. 10 is a flow chart for synthesizing and displaying a plurality of windows.

FIG. 11 is a flow chart of a normal line transfer without the α-blending.

FIG. 12A is an example of the display screen without the α-blending, and FIG. 12B is a memory map of the line memory in the line No. L.

FIG. 13 is a flow chart of the line transfer including the α-blending.

FIG. 14A is an example of the display screen with the α-blending, and FIG. 14B is a memory map of the normal line memory in the line No. L and the line memory for the α-blending.

FIG. 15 is a diagram showing the motion of the control data.

FIG. 16 is a diagram showing the transfer motion between buffer memories for transfer when the size is the same as the original without expansion, contraction and skip.

FIG. 17 is a diagram illustrating the contraction motion of the buffer memory for transfer.

FIG. 18 is a diagram illustrating the expansion motion of the buffer memory for transfer.

FIG. 19 is a diagram illustrating the skip motion of the buffer memory for transfer.

FIG. 20 is a diagram illustrating the motion of the buffer memory for transfer, in which expansion, contraction and skip exist together.

FIG. 21 is a diagram illustrating another motion of the buffer memory for transfer, in which expansion, contraction and skip exist together.

FIG. 22 is a diagram illustrating still another motion of the buffer memory for transfer, in which expansion, contraction and skip exist together.

FIG. 23 is a diagram illustrating a contraction motion at a certain magnification of the buffer memory for transfer.

FIG. 24 is a diagram illustrating an expansion motion at a certain magnification of the buffer memory for transfer.

FIG. 25 is a block diagram showing the display memory

section for storing the used line information.

FIG. 26A is an example of the display screen, FIG. 26B is the memory map and the output data of the line memory when the used line information is N, FIG. 26C is the memory map and the output data of the line memory when the used line information is N+2, and FIG. 26D is the memory map and the output data of the line memory when the used line information is N+4.

FIG. 27 is a diagram illustrating the motion when the background is repeatedly used.

The Best Modes of the Embodiments of the Invention

The preferred embodiments of the present invention will now be described with reference to the accompanying drawings.

FIG. 2 is a block diagram showing one embodiment of the programmable display device according to the present invention. This display device is composed of a main CPU 11, a main memory 12 for storing programs, display data and other data, a data processing circuit 13 which performs a processing for converting the display data in the main memory 12 into the data format for display, a display memory section 14 which stores the converted display data, an output processing circuit 17 which performs a processing for outputting the display data onto the screen, a DMA (Direct Memory Access) 18 which accesses to the data in the main memory 12, a program

memory 19, a data memory 20, a display processor 21 which interprets the command and data described in the program memory 19 and the data memory 20, and mainly performs transfer or the like of the display data according thereto, a sync signal generating circuit 22, and video inputs 23, 24.

The data processing circuit 13 comprises, as shown in FIG. 3, an YUV decoder 27a which performs YUV → RGB conversion with respect to the display data transferred from the display processor 19, a run length evolving circuit 27b which performs the run length evolvement with respect to said display data, a color extension circuit 27c for extending the color data with respect to said display data, a plurality of processing circuits of a plurality of color pallets 27d and 27e for performing the pallet conversion with respect to said display data, and a selector 28. The display memory section 14 comprises, as shown in FIG. 3, a data buffer 15 which can be used for storing the pattern data of a cursor, and a plurality of line memories 16 for storing the data display data and the used line information. The output processing circuit 17 comprises a selector for selecting an optional line memory from the plurality of line memories 16, an attenuator for changing the brightness of the display data in order to realize the α-blending and an adder for adding its output, a selector which is used for synthesizing the repeated background data, cursor and the like, and a D/A converter for

performing D/A conversion in order to display on the display, and the like. The display processor 21 has, as shown in FIG. 4, buffer memories for transfer, 25a, 25b, 26a and 26b.

This display device does not have a frame buffer for exclusive use, and takes the UMA (Unified Memory Architecture) structure which lodges the display data in the main memory 12, but it may have a structure that a frame buffer for exclusive use is included in the main memory 12.

The motion of this embodiment will now be described.

First, the general flow till the display data is actually displayed will be described.

The display data is stored mainly in the main memory 12 by the main CPU 11. These display data is read out by the DMA 18, and temporarily stored in the buffer memories 25a and 25b for transfer inside of the display processor 21 shown in FIG. 4. Then, after the display data is subjected to the motion such as expansion, contraction or skip and stored in the buffer memories 26a and 26b for transfer, the display data is converted to the data in a simple RGB format by the data processing circuit 13, and then stored in the line memory 16. The data written in the line memory 16 is read out for one pixel in conformity with the dot clock in the sync signal generated by the sync signal generating circuit 22. Then the data is subjected to the α-blending processing of two screens or synthesized with the repeated background data or cursor

by the output processing section 17, D/A converted, output to the display together with the sync signal and displayed. This is the general flow till the display data is actually displayed.

In this display device, the control of a considerable portion of the display is performed by the display processor 21. The display processor 21 has a program memory 19 and the data memory 20 for exclusive use, interprets the programs and data stored therein and performs motions such as transfer of the display data and the like. The information of the program memory 19 and the data memory 20 is transferred from the main memory 12 according to need. A plurality of programs/data are stored in the main memory 12 according to the display structure, the change of the graphic area and the like.

The command to transfer the display data from the main memory 12 may be issued directly from the main CPU 11 to the display processor 21 or may be issued from the display processor 21 itself. It is mainly when the display mode(bit number showing the information of one pixel) is changed that the main CPU 11 issues the transfer command. And it is mainly when the program/data required for forming one screen is larger than the RAM capacity of the display processor that the display processor 21 itself issues the transfer command. At this time, the program/data is replaced in the middle of the display.

With such a structure, the information can be transferred according to need, hence the display device can flexibly correspond to the screen mode or the change of the graphic area. In addition, a program or data exceeding the memory capacity can be executed. Thus, the RAM of the display processor may have a small capacity. Accordingly, construction of a compact or a low-cost system becomes possible.

Moreover, when the motion of the display processor 21 is set and there is no need of change, the program memory 19 or the data memory 20 may be ROM. In this case, it is not necessary to transfer the data from the main memory 12. Since the ROM can have a smaller chip area compared to that of the RAM having the same capacity, it is advantageous from the standpoint of cost.

Next, the basic motion of the display processor 21 when a program is given to the display processor 21 to perform the screen display will be described. FIG. 5A ~ FIG. 5C are diagrams illustrating the display data of the main memory 12 and the display output of the display. All of them are for storing the display data stored preliminarily in the main memory 12 in the line memory 16. Now explanation will be made for a case where a beta screen is displayed and a case where a number of windows and the like are synthesized and displayed.

The beta screen means that backgrounds, cursor, windows and the like are stored preliminarily in the main memory 12 as a synthesized beta screen data by the main CPU 11, as shown in FIG. 5A, and when the display is performed, the beta screen data is read out sequentially from the top address and transferred to the line memory 16.

When a number of windows are synthesized, there are two cases that the α-blending is not considered (see FIG. 5B) and that the α-blending is considered (see FIG. 5C). The α-blending means a semi-transparent synthesis, and for example, when two windows are superposed, only the window of this side in the superposed portion is normally displayed. But if the α-blending is set, the window of this side becomes transparent, and the window of back side can be seen. In other words, the α-blending means a function to synthesize a plurality of display data at a certain percentage and display them. On the other hand, the motion of the display processor 21 is related to the motion of expansion, contraction and skip, and the control of the data processing circuit 13 and the used line information, but these motions will be described later.

Next, the motion of the display device when these screen displays are performed will be described. FIG. 6 is a flow chart for displaying the beta screen data for one screen. FIG. 7 shows an example of the display screen at that time, and FIG. 8 shows a memory map of the main memory 12 in which the

beta screen data is stored. First, in order to display one screen, in Step A1, the coordinate size x1 in the X direction of the beta screen data and the coordinate size y1 in the Y direction thereof are obtained.

Then, in Step A2, the top address beta_addr which stores the beta screen data in the main memory 12 is obtained as the top address addr which stores the beta screen corresponding to the line No. L. These data can be obtained as the immediate data which are fixed in the program, if they are fixed data. Furthermore, if they have optional sizes, these data existing in the main memory 12 may be obtained by transferring these data to the data memory 20 and referring to the data memory 20. In Step A3, the next horizontal line number following the horizontal line number now being displayed is obtained as the line No. L, and it is judged whether this value is even or odd in Step A4. Then, the data transfer in the x1 size is carried out from the top address addr which stores the beta screen data corresponding to the line No. L in the main memory 12 to the line memory 16a in Step A5 if it is even, or to the line memory 16b in Step A6 if it is odd.

The reason why the write to the line memory 16a and the line memory 16b is switched by the even and odd line numbers is that when the line memory is accessed on the display side, the access thereto is not possible from the display processor 21. By providing another line memory separate from the line

memory being used for the display, the display processor 12 can access to the line memory even during the display.

After the data is transferred to the line memory 16a or the line memory 16b, in Step A7, the coordinate size y1 in the Y direction of the beta screen and the line No. L which is displayed next are compared. If the value of (L+1) is smaller than y1, in Step A8, the top address addr which stores the beta screen data corresponding to the line No. L is added by the coordinate size x1 in the X direction of the beta screen to obtain the top address addr which stores the beta screen corresponding to the next line number. The weight for synchronism (Step A9) controls the overwrite to the line memory by judging if the line memory 16a or the line memory 16b now being used for the display is still being used or not, that is, by writing to the line memory after waiting till the next horizontal display starts. It becomes possible to display for one pixel by performing transfer to the line memory 16 a or the line memory 16b described above y1 times.

Next, the description will be for the case where a plurality of windows and the like are synthesized and displayed.

In the display of the beta screen, the display data in the main memory 12 is sequentially read out from the top address and displayed, but the data at an optional position in the main memory 12 can be displayed in an optional

combination by taking out an optional number of data, according to the program given to the display processor 21. For example, in the case of the window system, the display data of a plurality of windows are stored in the main memory 12 in a completed form in separate addresses, respectively, and according to the position of each window and the priority thereof, they can be displayed on a real time basis by superposing them.

Here, it is assumed that, as shown in the memory map of FIG. 9, various display data such as the background data, the cursor data, the window 1 data, the window 2 even data, the window 2 odd data and the like are stored in a completed form in optional address positions in the main memory 12. Among these display data, only the data which is displayed when it is synthesized is read out and transferred to the line memory. The window 2 even data and the window 2 odd data mean the data structures which are taken in as the even data and as the odd data per field when the interlace signal such as NTSC signal is taken in on the main memory 12. However, the display of the cursor will be described later.

FIG. 10 is a flow chart for synthesizing and displaying a plurality of windows. It shows a motion that only the data displayed when the various data in FIG. 9 are synthesized and read out to display for one screen.

Since the display data such as window coordinates,

priority and the like are optional data which may be changed at any time, every time one screen is displayed, the data transfer from the main memory 12 to the data memory 20 is performed by the display processor 21 in Step B1. In addition, in order to display one screen, the coordinate size y1 in the Y direction of the screen is obtained in Step B2, and the next horizontal line number following the horizontal line number now being displayed is obtained as the line No. L in Step B3. In Step B4, it is judged if it is subjected to the α-blending or not, and if the α-blending is not to be carried out, the normal line transfer is performed (Step B5), and if the α-blending is carried out, the α-blending line transfer is performed (Step B6). Next, in Step B7, the line No. L which is to be displayed and the coordinate size y1 in the Y direction of the screen are compared, and if the loop of y1 times is not completed, the processing of the weight for synchronism (Step B8) which controls the overwrite into the line memory is performed, and the display for one screen is performed by performing the above processing for y1 times.

FIG. 11 is a flow chart of a normal line transfer without the α-blending.

FIG. 12A is an example of the display screen without the α-blending, and FIG. 12B is a memory map of the line memory in the line No. L. Assuming that the line No. L in FIG. 12 is the line No. L to be displayed next, the normal line transfer

on the line number will be described. In Step C1, the display processor 21 calculates the boundary point between respective display data on the line No. L without the α-blending and the point number. The display data of each window is transferred to the data memory 20, and the boundary points and the point number are calculated from the upper right coordinate, the lower left coordinate, the coordinate size in the X direction, the coordinate size in the Y direction, the priority and the like. Alternatively, the data calculated in advance by the main CPU 11 is transferred to the data memory 20, and the data may be obtained only by referring to the data memory 20.

The boundary point at this time is defined as xpt [ ] (in the [ ], a number showing the sequence order is entered), and the number of the boundary points is defined as xpm. As shown in FIG. 12A, the boundary points on the line No. L will be xpt [0] = xs0, xpt [1] = xs1, xpt [2] = (xe1 + 1), xpt [3] = (xe2 + 1), xpt [4] = (xe0 + 1), and the number of boundary points xpm will become 5. In Step C2, the boundary counter xp is cleared, and in Step C3, the left boundary point xpl on the line L is obtained, and in Step C4, the right boundary point xpr nearest to the left boundary point is obtained. The display data between these xpl and xpr is judged, and in Step C5, the top address addr which stores the display data corresponding to the line No. L is obtained. Initially, xpl

= xpt [0] = xs0, and xpr = xpt [1] = xs1, therefore, it can be judged that this display data is the background data, and the top address addr which stores the background data corresponding to the line No. L can be obtained from addr = back_addr + x1*L + xs0.

In Step C6, it is judged if the line No. L is even or odd, and the data transfer to the line memory 16a (Step C7) or the data transfer to the line memory 16b (Step C8) is switched. The size of the data transfer to the line memory 16a and the line memory 16b becomes xpr - xpl, since the display area is xpl, xpr - 1. Since the write position into the line memory 16a and the line memory 16b is xpl, the data transfer to the line memory 16a or the line memory 16b means that the data of (xs1 - xs0) is transferred from addr to xs0 of the line memory 16a or the line memory 16b. The right boundary point xpr becomes the left boundary point xpl when the next data between xs1 and (xe1 + 1) is transferred, in Step C9, the left boundary point xpl can be obtained by making xpl = xpr. Then by moving to obtain the right boundary point xpr (Step C4) described above, and these motions are similarly performed between the boundaries xs1 and (xe1 + 1), (xe1 + 1) and (xe2 + 1), and (xe2 + 1) and (xe0 + 1), the data transfer of one line of the line No. L can be done. In Step C10, the boundary count xp and the boundary point number xpm are compared, and when the boundary count xp becomes the same with

or larger than the boundary point number xpm, the processing of the next line is started.

FIG. 13 is a flow chart of the line transfer including the α-blending. FIG. 14 shows an example of the display screen including the α-blending. FIG. 14A is an example of the display screen of the α-blending, and FIG. 14B is a memory map of the normal line memory in the line No. L and the line memory for the α-blending. The α-blending line transfer on the line number, assuming the line No. L in FIG. 14 as the line No. L to be displayed next, will now be described. In Step D1, the display processor 21 calculates the boundary point between respective display data on the line No. L with the α-blending and the point number. The boundary point number is increased by 1 that the normal display screen example in FIG. 12. The boundary point and the point number are calculated from the upper right coordinate, the lower left coordinate, the coordinate size in the X direction, the coordinate size in the Y direction, the priority and the like. Alternatively, the data calculated in advance by the main CPU 11 is transferred to the data memory 20, and the data may be obtained only by referring to the data memory 20.

The boundary points on the line No. L will be xpt [0] = xs0, xpt [1] = xs1, xpt [2] = xs2, xpt [3] = (xe1 + 1), xpt [4] = (xe2 + 1), xpt [5] = (xe0 + 1), and the number of boundary points xpm will become 6. Since the boundary without the

α-blending is the same as the normal line transfer, the case of the boundary counter xp with the α-blending will be described. The left boundary point xpl on the line L obtained in Step D14 will be xpl = xpr = xpt [2] = xs2, and xpr = xpt [3] = (xe1 + 1) by the acquisition of the right boundary point xpr in step D4. The top address addr which stores the window 1 data corresponding to the line No. L of this display data is calculated as addr = win1_addr + (xe1 - xs1 + 1) * (L - ys1) + (xs2 - xs1) (Step D5). It is then judged if the line No. L is even or odd in Step D6, and the data transfer to the line memory 16a (Step D7) or the data transfer to the line memory 16b (Step D8) is switched.

The size of the data transfer to the line memory 16a or the line memory 16b will become xpr - xpl, since the display area is xpl, xpr - 1. Since the write position into the line memory 16a and the line memory 16b is xpl, the data transfer to the line memory 16a or the line memory 16b means that the data of ((xe1 + 1) - xs2) is transferred from addr to xs2 of the line memory 16a or the line memory 16b. After the completion of the data transfer, it is judged if there is another data to be α-blended or not with respect to the data in Step D9. In this case, the window 1 and the window 2 are to be α-blended, and the top address addr which stores the window 2 even data corresponding to the line No. L of this display data is calculated as addr = win2e_addr + (xe2 - xs2

+ 1) * (L - ys2)(Step D10).

It is then judged if the line No. L is even or odd in Step D11, and the data transfer to the line memory 16c (Step D12) or the data transfer to the line memory 16d (Step D13) is switched. The line memory 16c and the line memory 16d at this time are line memories for the α-blending. The size of the data transfer to the line memory 16c and the line memory 16d becomes xpr - xpl, since the display area is xpl, xpr - 1. Since the write position into the line memory 16c and the line memory 16d is xpl, the data transfer to the line memory 16c or the line memory 16d means that the data of (xel + 1) - xs2) is transferred from addr to xs2 of the line memory 16c or the line memory 16d. Normally, the line memory can have the data not to be α-blended, and the line memory for the α-blending can have the data to be α-blended, separately, to make it possible to perform the synthesized display by the α-blending processing of the hardware. The following processing in the Step D14 and Step D15 is the same as the normal line transfer.

The display of the cursor can be also displayed by the motion procedure described above, but it is also realized by providing the coordinates of the cursor, the size in the X direction of the cursor, the size in the Y direction of the cursor, the top address curs_addr for storing the cursor data and the like after the transfer of the display data for one

line to the line memory, and finally synthesizing and displaying them. When the display is made on the data of the α-blending, the cursor can be displayed by writing into both the normal line memory and the line memory for the α-blending. In this method, the cursor is always the top priority, and the processing speed can be increased. The basic motion of the display processor 21 has been described above.

Next, other motions performed by the display processor 21 will be described.

First, the processing of expansion, contraction and skip of the display data will be described. As shown in FIG. 4, the display processor 21 has two sets of the buffer memories for transfer therein. The display data read in from the main memory 12 is stored in the first set of the buffer memories for transfer 25a and 25b, and then stored in the other set of the buffer memories for transfer 26a and 26b, and thereafter stored in the line memory 16 for display. The readout and write between the buffer memories for transfer can be precisely controlled by the program provided to the display processor 21.

Specifically, processing can be done at an optional position per unit of a pixel, such as start/stop of the readout counter of the first set of the buffer memories for transfer 25a and 25b (referred to as "readout memory"), start/stop of the write counter into the other set of the buffer memories

for transfer 26a and 26b (referred to as "write memory"), and whether the write is done or not, enabling the expansion or contraction of the display image, the expression that a right-hand side image from a certain position is slipped in the right direction and it looks like there is a hole in the image (referred to as "skip") and the change to the display data in which those are mixed become possible.

The motion of the expansion, contraction and skip are controlled as shown in the diagram illustrating the motion of the control data in FIG. 15. The control data has 2 bits information for one pixel, and controls the readout counter and the write counter between the buffer memories 25a, 25b, 26a and 26b for transfer, or if the write is to be done or not, for each pixel unit. FIG. 16 is a diagram showing the transfer motion between the buffer memories for transfer when the size is the same as the original without expansion, contraction and skip, and in this case, "00" is continuously provided as the control data. Then, both the readout counter and the write counter are counted up by 1 continuously and the same data as the readout memory is written in the write memory, thus the data is transferred in the same size.

When the data is contracted, provide "01" to the data corresponding to the pixel you want to omit in the control data. In FIG. 17 showing the contraction motion, the display data is written sequentially up to 0, 1, 2 and 3 into the write

memory, but since the control data at a position 3 is "01", the write counter stops, and the data 4 is overwritten on the position 3. Thereby, the display data is contracted by one pixel. If the control data is set to "01" every other pixel, the horizontal direction of the image is contracted to 1/2, and if the rate to set "01" is changed partially, for example, the image becomes cylindrical shape.

When the data is expanded, "10" is set to the corresponding position of the control data. In FIG. 18, the display data is written sequentially up to 0, 1, 2 and 3 into the write memory, but since the control data at a position 3 is "10", the readout counter stops, and the data 3 is rewritten again to the next position of 3. Thereby, the display data is expanded by one pixel.

When the control data is "11", it is skipped. In FIG. 19, up to 0, 1 and 2, the data is written as it is, but since the control data of position 3 is "11", the readout address stops. Hence, the display data of position 3 is written in the next pixel on the right side. In addition, write to the write memory is not performed, and nothing is written in the position 3 of the write memory. Thus, the skip for one pixel is performed.

As described above, by setting the value of the control data, expansion, contraction and skip are possible. Furthermore, by setting the expansion, contraction and skip

in combination, as shown in FIG. 20 to FIG. 22, the display data is expanded partially, and contracted partially, thus a complicated modification of the display data is possible.

In many cases, the expansion and contraction rate is constant in the horizontal direction, and in these cases, the control data is repeated in the same pattern. In the present embodiment, by setting the repeated patterns and the repeated points, the expansion, contraction and the like can be specified with a fewer data compared to the case where the control data for one horizontal line is written. For example, when the data is contracted to 0.75 times, the control data will be repeated in the order of "00", "00", "00" and "01", as shown in FIG. 23. In this case, by setting the control data for 4 pixels and the repeated point so that repetition is performed per a unit of 4 pixels, the same control data is repeatedly used to perform the contraction motion. FIG. 24 shows the case where the data is expanded similarly to 1.75 times.

In the present embodiment, 2 kinds of video input are provided, and the display processor 21 can take in the video image data thereby. The video image signal is stored in the line memory for the video input, after being A/D converted. There are two line memories for the video input per one kind of video input, and they are used for readout and for write by switching alternately, as in other line memories. The

video data written in the line memory for the video input is read out by the display processor 21, and after being subjected to the processing of expansion, contraction and skip, transferred to the line memory 16.

Next, the data processing circuit 13 will be described. The display data stored in the main memory are stored not only in a normal RBG format but also in various data format. While the display data is read out from the main memory 12 by the display processor 21 and written into the line memory 16, the display data in various kinds of data formats are converted to the RBG format through the processing circuits, such as the YUV decoder 27a, the run length evolving circuit 27b, the color extension circuit 27c and the color pallet 27d, 27e, and stored in the line memory 16. The display processor 21 instructs the selector 28 which data processing circuit is to be selected for the conversion for every pixel. There can be a plurality of color pallets, and for example, a pallet can be changed for every window. Moreover, other data processing circuits may be added, thereby the display processor 21 can correspond to various formats of the display data.

The display data past through the data processing circuit 13 is written in the line memory 16, but some values among the display data can be set as a write-through data which is not actually displayed. When the display processor 21

transfers the display data from the main memory 12 and the data buffer 15 to the line memory 16, if there is the write-through data, the pixel of that portion is not written in the line memory 16. It is effective for the display of an image which is not a rectangle, for example, a mouse cursor.

Next, the motion for displaying a screen by using the used line information will be described. Normally, the line memories for display function in a pair. This is because the display processor 21 cannot access for the write to the line memory which is now performing readout for the display, thus the display processor 21 writes the display data in the next line to the other line memory independent from the line memory which is now performing readout. Every time the line to be displayed is changed, the line memories which perform readout and write are alternately switched to continue the display. However, when a plurality of screens are synthesized and displayed, as shown in FIG. 5B and FIG. 5C, and when the background is not particularly displayed, in some cases, write of the display data into the line memory is only performed with respect to the portion where the window is displayed, and the display data of the former line remains in other portions. Therefore, it is required to clear the line memory before the write, and the time for clearing becomes necessary. The used line information makes it unnecessary to clear the line memory.

The used line information corresponds to the display data of each pixel on the line memory at a ratio of 1:1, and shows in which line the display data is used. The used line information corresponding to one pixel of the display data is more than the bit numbers (if the screen size is 1280 x 1024, 11 bits) which can express (the number of pixel in the vertical direction of the screen + 1), and for the same numbers of the pixels as the display data in each line memory, that is, for the numbers of the horizontal pixels.

FIG. 25 is a block diagram showing the display memory section 14 for storing the used line information. To the line memories 16a ~ 16f are connected comparators 31 ~ 36 and AND circuits 37 ~ 42, respectively. The line memories 16e and 16f are the memories to store the background data described below. The comparators 31 ~ 36 compare the display line numbers and the used line information, and if the values agree, output the theoretical value 1, and if the values do not agree, output the theoretical value 0. The AND circuits 37 ~ 42 output the display data as it is when the theoretical value 1 is input, and do not output the display data when the theoretical value 0 is input.

Now, the motion to display the screen will be described based on FIG. 26. FIG. 26A is an example of the display screen, FIG. 26B is the memory map and the output data of the line memory when the used line information is N, FIG. 26C is the

memory map and the output data of the line memory when the used line information is N+2, and FIG. 26D is the memory map and the output data of the line memory when the used line information is N+4. As shown in FIG. 26B, while the display of the (N - 1)th line is being performed, the display processor 21 writes the display data of the Nth line in the line memory. In the Nth line, there is window 1, and while the display data of the window 1 is written, N is simultaneously written in the used line information. When the Nth line is displayed, the line number N which is being displayed and the used line information are compared for every pixel of the line memory, and only when they are identical, it is considered that the display data is effective, and the display data in the line memory is output.

The write into the same line memory is done in the (N + 2)th line, because the two line memories are used alternately. As shown in FIG. 26C, in the (N + 2)th line, there are window 1 and window 2, and (N + 2) is written into the display data and the used line information. Thus, the display is performed.

Next, the write of the (N + 4)th line is performed. The (N + 4)th line is only for window 2, and as shown in FIG. 26D, (N + 4) is written into the display data and the used line information. At this time, the data of window 1 which was written in the (N + 2)th line remains, and if processing is

carried out without taking any particular measure, the above will be displayed, subsequently a wrong display comes out. In the present embodiment, however, the used line information of the portion of the old window 1 remains (N + 2) which subsequently is ignored, and only the window 2 is displayed correctly.

The display for all lines are performed as described above, it is required to clear the used line information of all the line memories for every vertical retrace period. It is to prevent the display data of the previous vertical display period from being displayed. Clearing is performed by writing an unused value as the used line information.

Next, the repeated display of the same pattern will be explained. As is often seen in the background screen of the window system, sometimes the same pattern is repeatedly displayed in the horizontal direction. In this case, by making it possible to loop the readout address read out from the line memory 16 in an optional range, a particular pattern can be repeatedly displayed. Thereby, in particular, in the case where the background data is stored in the main memory 12, the data volume to be read out can be reduced, hence the traffic of the data bus of the main CPU 11 can be reduced. When using this function, it is necessary to have a pair of line memories 16e and 16f for exclusive use for storing the repeated pattern other than the normal line memories.

Therefore, it is necessary that the line memories are at least 4, and when the α-blending is simultaneously used, at least 6. This repeated display function of this specific pattern will now be described.

FIG. 27 is a diagram illustrating the motion when the background is repeatedly used. When the data of the Nth line is written to the line memory, first the display data of the window and the used line information N are written in the line memory which stores the window data, as in the normal case. Next, the display data of the background and the used line information N are written in the line memory which stores the background data, and the repeated point is set. There are several methods to set the repeated point, such as a method to provide a register for exclusive use, to write a value dinstinguishable from the normal case into the used line information and the display data, or to prepare a line memory for exclusive use.

In order to display, first compare the used line information in the line memory for storing the window data with the line number being displayed. If they agree, the display data of the window is output, and if they don't agree, the background data is output. Though the background data is not shown, the background data shown by the background data readout counter inside thereof is output. If the value of this readout counter agrees with the value of the repeated

point, the value of the readout counter is cleared. The background data output thereby returns to the initial stage of the line memory for storing the background data, and the background data is output repeatedly.

Next, the data buffer 15 will be described. Normally, the display data is stored in the main memory 12, but the display data in which the size of cursor is small, and the pattern is set may be stored in the data buffer 15. The display data stored in the data buffer 15 can be written in the line memory 16 by the display processor 21. Moreover, the display data can be transferred not to the line memory 16, but to the program memory 19 or the data memory 20 of the display processor 21, or the main memory 12, therefore, the display data can be used for the general purpose, not limited to the display of the cursor.

Furthermore, there are several methods to set the combination ratio of two screens by the α-blending. One of them is to prepare a register for exclusive use which stores the combination ratio and read out the combination ratio from the register at the time of α-blending. In this case, it is necessary for the display processor 21 to rewrite the content of the register every time the combination ratio is changed. Another method is to prepare a LUT which stores a plurality of combination ratio, and write the display data together with the call address of the LUT for every pixel,

and the other method is to write the combination ratio directly to the line memory for every pixel.

Industrial Applicability

According to the invention of the aspect 1, the display data of the portion required at the time of display is taken out from the main memory and used. Therefore, it is possible to take out the data at an optional position in the main memory and combine them optionally. This control is performed by the display control section, thus the processing load of the main control section in the software can be reduced when a plurality of windows are simultaneously displayed on the screen. Hence, the speed of movement and switching of each window can be increased.

According to the invention of the aspect 2, when the data in the line memory is read out, and if the data is to be repeated in the line direction (as the background in the window system), the readout line memory address can be looped in an optional position. Hence, redundant processing is not necessary and the processing can be performed at a high speed.

According to the invention of the aspect 3, since the cursor and the repeated background can be stored in the data buffer memory, it is not necessary to read out the routine data from the main memory. Thus, the load of the data bus can be reduced, redundant processing is not necessary and the

processing can be performed at a high speed.

According to the invention of the aspect 4, it is not necessary to perform the expansion/contraction processing with respect to the data for the display in advance, since the expansion/contraction processing is performed when the display data is read out, hence the efficiency of using the bus can be increased. In addition, when the video input picture is displayed, it is normal that the change of the picture size is required, but by performing the expansion/contraction processing at the output stage, the expansion/contraction circuit can be utilized more effectively. Thereby, while taking in the video data always in a full size, the display can be set in an optional size without the need of transferring the data to the frame memory or the like.

According to the invention of the aspect 5, expansion and contraction at a certain magnification can be performed with a simple processing, by repeating the stop/motion of the readout address count from the first buffer memory in a predetermined order, hence the processing can be performed at a high speed.

According to the invention of the aspect 6, since the display control section can perform the data conversion based on the data format information in the stored information, the format to store the data for the display is not limited. Hence

there is no need to transfer the display character and the like stored in the data memory to the frame buffer, thus the processing can be performed at a high speed.

According to the invention of the aspect 7, since said display control section is provided with a program memory and a data memory for storing the necessary program and the data, it is not necessary to read out the data from the main memory every time of processing. Hence, the number to use the data bus can be reduced, thus the processing can be performed at a high speed.

According to the invention of the aspect 8, said display control section can flexibly correspond to the change of the screen mode or the graphic area so as to transfer the information necessary for said program memory and said data memory from the main memory. Since the program or the data exceeding the capacity can be read out from the main memory, the capacity of the memory may be small, thus a compact system can be built at a low cost.

According to the invention of the aspect 9, when the display data is transferred to each line memory, the line number which used the data is written simultaneously in the used line information memory corresponding to every one dot, and it is judged if the data on the line memory is effective or not by comparing it with the line number which is to be displayed at the time of display, thereby it is not required

to clear the content of the line memory every time the line memory is used, hence the processing can be performed at a high speed. And the used line information in the line memory does not have to be deleted for every line display but has only to delete the used line information in all the line memory for every period of vertical retrace, hence the processing can be performed at a high speed.

CLAIMS

1. A programmable display device comprising:

a main memory which stores the display data;

a data processing circuit which converts the data format of said display data into the data format of the screen display;

a number of line memories which store the display data converted by said data processing circuit per unit of the display line;

a display control section which controls the transfer and storage of the display data from said main memory to/in said line memory and the readout of the necessary display data from said line memory to display it on the screen; and

a main control section which controls the storage of said display data in said main memory, and the transfer of the stored information including the data format and the storage address to said display control section, wherein

said display control section reading out said display data by specifying the address of the display data for one line which has a possibility to be displayed on the screen to said main memory from which the display data is transferred, based on said stored information, causing said data processing circuit to perform the data transfer and select said line memory to store said display data.

2. A programmable display device according to claim

1, wherein said display control section controls the storage of the display data to be utilized repeatedly in said line memory, so that when the repeated display data is displayed, said repeated display data is read out from said line memory by specifying the address thereof and displayed on the screen.

3. A programmable display device according to claim 1, further comprising a data buffer memory for storing the display data to be utilized repeatedly, and when said data is displayed on the screen, said display control section causes said repeated display data to be read out from said data buffer memory and displayed on the screen.

4. A programmable display device according to claim 1, which includes:

a first buffer memory for storing the display data read out from said main memory;

a second buffer memory for storing the display data read out from said first buffer memory; and

an address counter for counting the readout address and the write address of said first and the second buffer memories; wherein

said display control section controlling the stop and motion of the readout address count and the write address count, respectively, with respect to said address counter, performing the processing of expansion, contraction and skip and storing the data in said line memory.

5. A programmable display device according to claim 4, wherein said display control section causes the stop and motion of the readout address count to be repeated in a predetermined order.

6. A programmable display device according to claim 1, wherein said data processing circuit has a plurality of conversion processing circuits for converting various data formats, and

said display control section selects said conversion processing circuits based on the data format information of said stored information.

7. A programmable display device according to claim 1, wherein said display control section is provided with a program memory and a data memory for storing the necessary programs and data.

8. A programmable display device according to claim 7, wherein said display control section causes the information necessary for said program memory and said data memory to be transferred from said main memory.

9. A programmable display device according to claim 1, wherein said display control section adds the line information showing in which line the data is to be used when storing the display data in said line memory, and controls the display of the data in such a manner that when reading out the display data from said line memory, the line

information is read out simultaneously and the data is displayed only when the line which uses said display data is the same with the line information.

ABSTRACT

It comprises a main CPU, a main memory for storing the programs, display data and other data, a data processing circuit for performing a processing to convert the display data in the main memory to the data format for the display, a display memory section for storing the converted display data, an output processing circuit for performing a processing to output the display data on the screen, a DMA for performing a data access to the main memory, a program memory, a data memory, a display processor for interpreting the commands/data described in the program memory and the data memory and transferring the display data according thereto, and a sync signal generating circuit.

1152-237P

IN THE U.S PATENT AND TRADEMARK OFFICE

Applicant: Satoshi NAKAMURA et al.

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Serial No.: New

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Title: PROGRAMMABLE DISPLAY DEVICE

L E T T E R

Assistant Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

July 15, 1999

Sir:

Attached hereto are 2 sheet(s) of corrected Formal Drawings. Please substitute these drawings for the corresponding 2 sheet(s) of drawings on file in the above-identified application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fee required under 37 C.F.R. § 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By

CHARLES GORENSTEIN
Reg. No. 29,271
P.O. Box 747
Falls Church, VA 22040-0747

CG/tnp
Enclosures: Figure 10 and Figure 13

FIG. 10

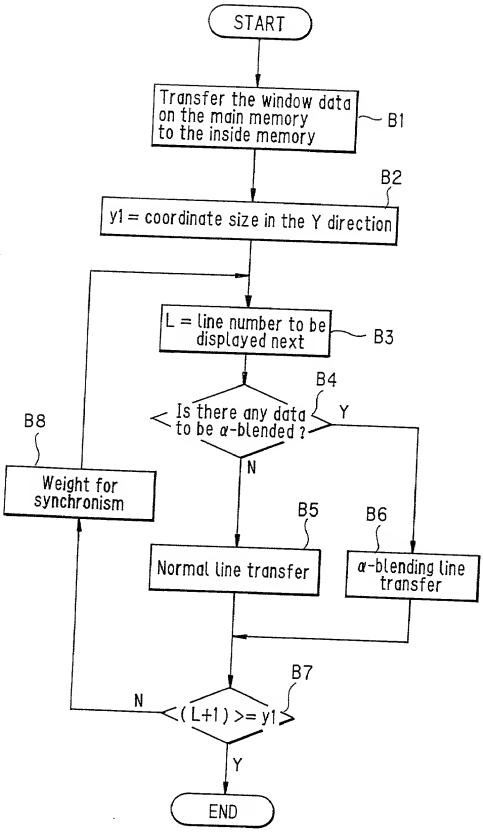

START
Transfer the window data on the main memory to the inside memory
B1
B2
y1 = coordinate size in the Y direction
L = line number to be displayed next
B3
B4
Is there any data to be α-blended ?
Y
N
B8
Weight for synchronism
B5
B6
Normal line transfer
α-blending line transfer
B7
N
(L+1) >= y1
Y
END

FIG. 13

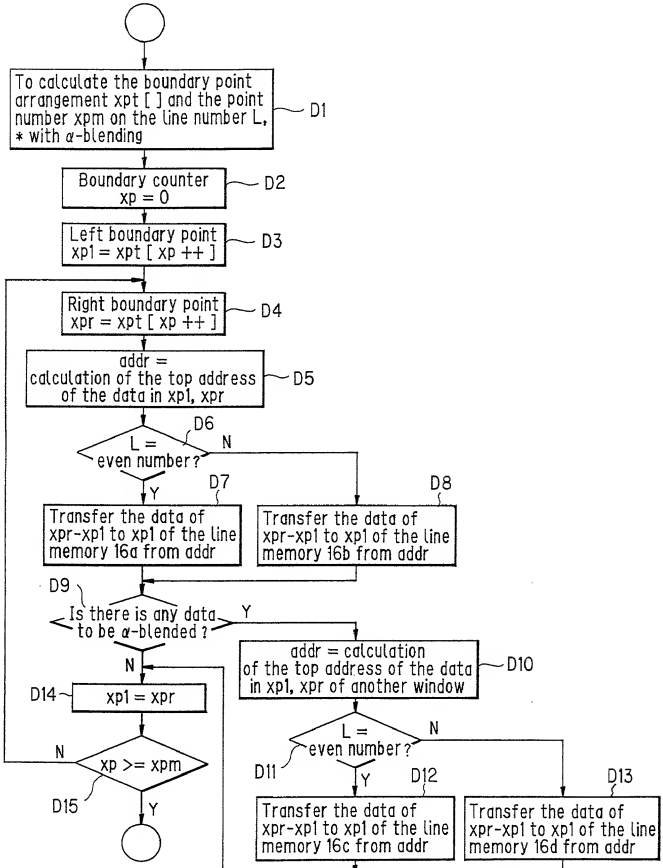

To calculate the boundary point arrangement xpt [ ] and the point number xpm on the line number L, * with α-blending
D1
Boundary counter xp = 0
D2
Left boundary point xp1 = xpt [xp ++]
D3
Right boundary point xpr = xpt [xp ++]
D4
addr = calculation of the top address of the data in xp1, xpr
D5
L = even number?
D6
N
Y
Transfer the data of xpr-xp1 to xp1 of the line memory 16a from addr
D7
Transfer the data of xpr-xp1 to xp1 of the line memory 16b from addr
D8
Is there is any data to be α-blended ?
D9
Y
N
addr = calculation of the top address of the data in xp1, xpr of another window
D10
xp1 = xpr
D14
L = even number?
D11
N
Y
Transfer the data of xpr-xp1 to xp1 of the line memory 16c from addr
D12
Transfer the data of xpr-xp1 to xp1 of the line memory 16d from addr
D13
xp >= xpm
D15
N
Y

FIG. 1

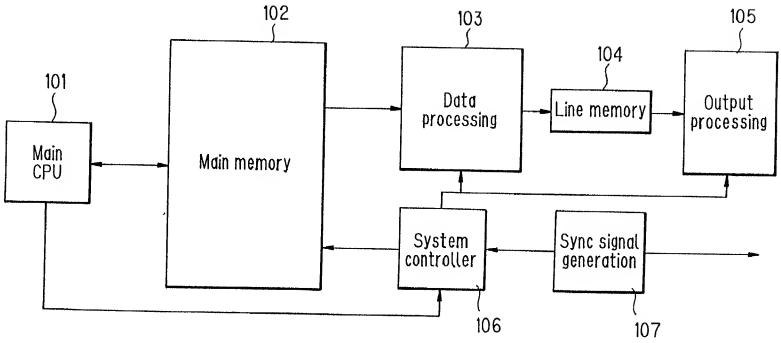


FIG. 2

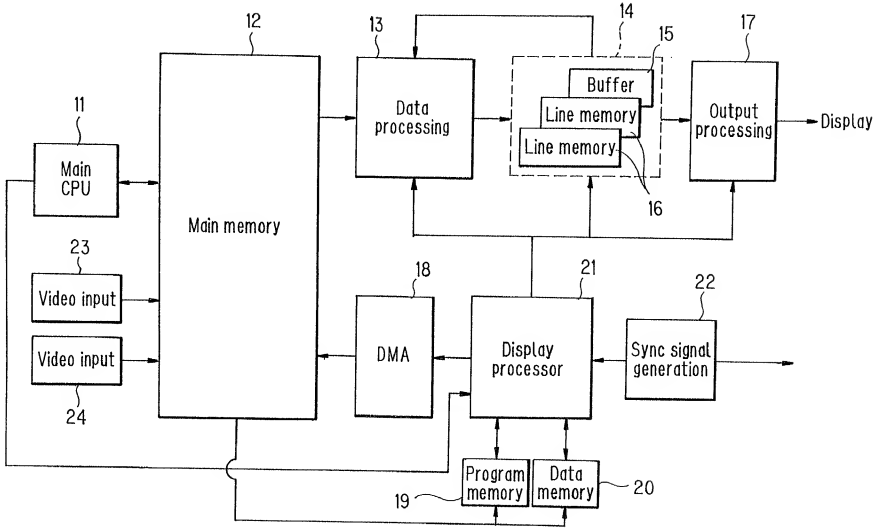


FIG.3

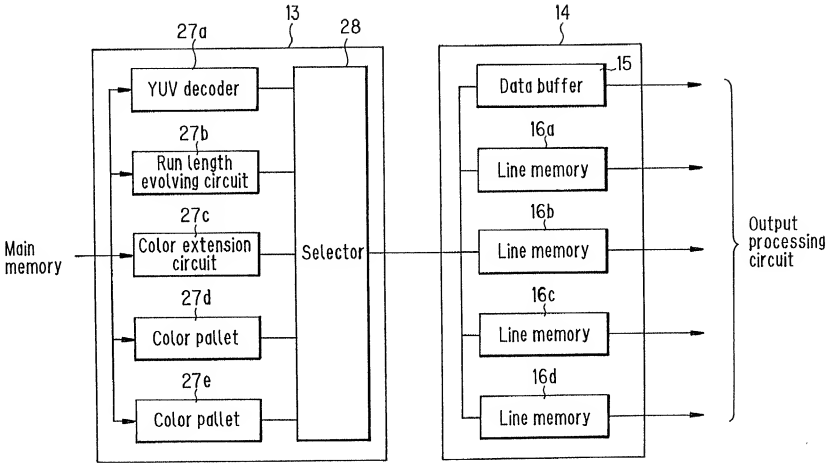


FIG. 4

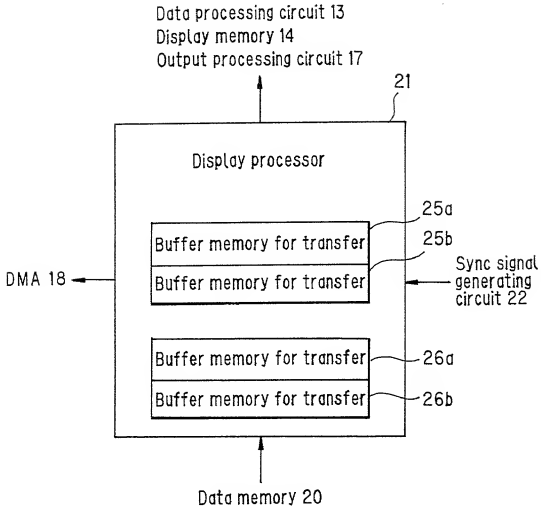

Data processing circuit 13
Display memory 14
Output processing circuit 17
21
Display processor
25a
Buffer memory for transfer
25b
Buffer memory for transfer
DMA 18
Sync signal generating circuit 22
Buffer memory for transfer
26a
Buffer memory for transfer
26b
Data memory 20

FIG. 5A

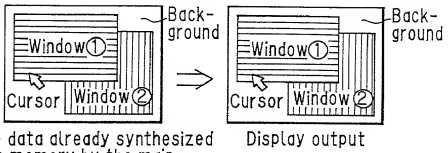
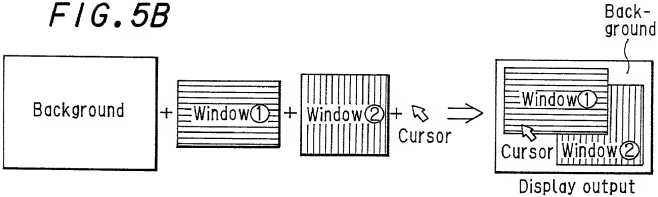


Image data already synthesized on the memory by the main processor

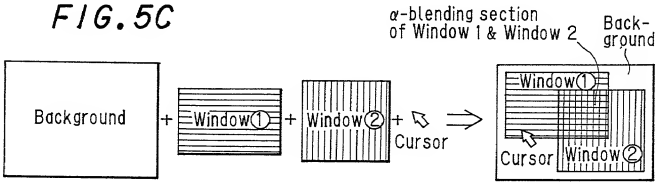
Display output

FIG. 5B



Display output

FIG. 5C



Display output

FIG.6

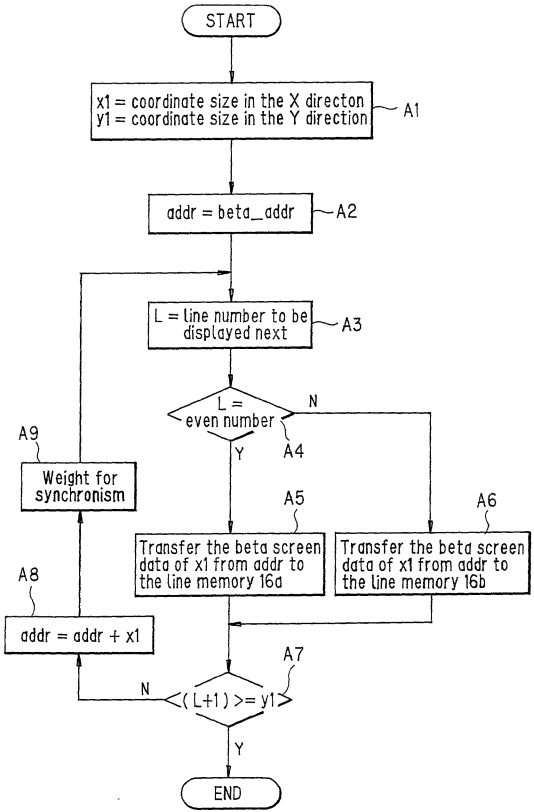

START
x1 = coordinate size in the X directon
y1 = coordinate size in the Y direction
A1
addr = beta_addr
A2
L = line number to be displayed next
A3
L = even number
N
Y
A4
A9
Weight for synchronism
A5
Transfer the beta screen data of x1 from addr to the line memory 16a
A6
Transfer the beta screen data of x1 from addr to the line memory 16b
A8
addr = addr + x1
A7
N
(L+1) >= y1
Y
END

FIG. 7

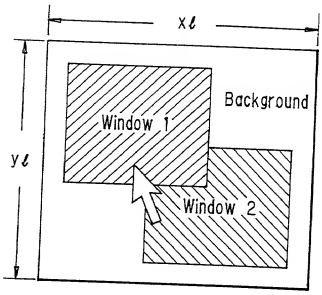

xℓ
yℓ
Background
Window 1
Window 2

FIG. 8

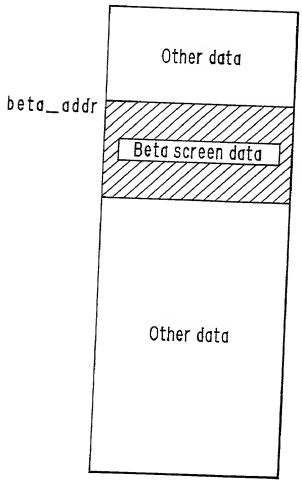

Other data
beta_addr
Beta screen data
Other data

FIG. 9

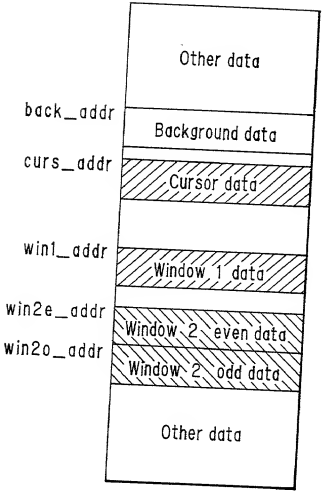

Other data
back_addr
Background data
curs_addr
Cursor data
win1_addr
Window 1 data
win2e_addr
Window 2 even data
win2o_addr
Window 2 odd data
Other data

FIG. 10

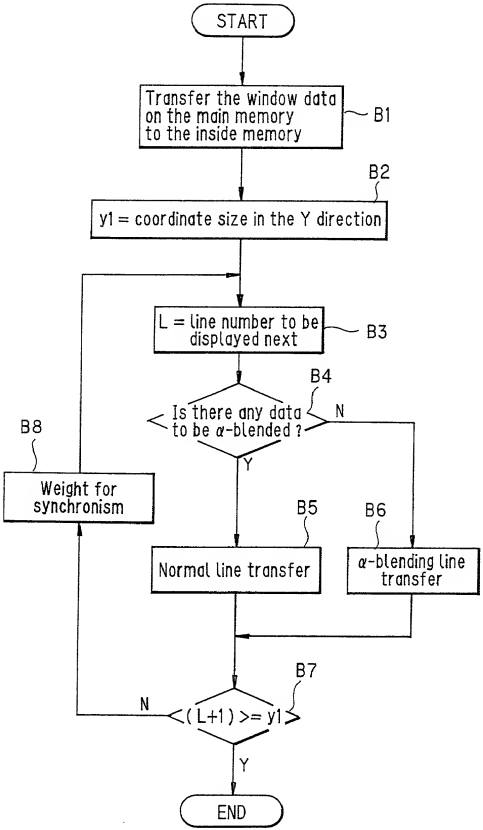

START
Transfer the window data on the main memory to the inside memory
B1
B2
y1 = coordinate size in the Y direction
L = line number to be displayed next
B3
B4
Is there any data to be α-blended ?
N
Y
B8
Weight for synchronism
B5
B6
Normal line transfer
α-blending line transfer
B7
N
(L+1) >= y1
Y
END

FIG. 11

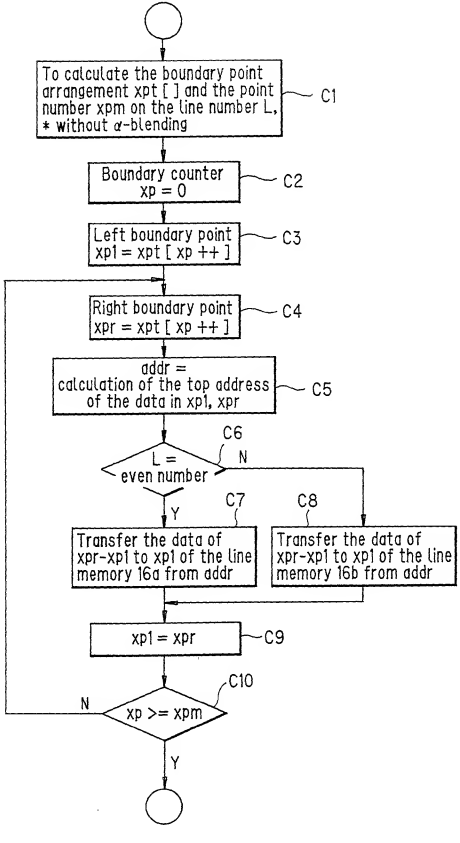

To calculate the boundary point arrangement xpt [ ] and the point number xpm on the line number L, * without α-blending
C1
Boundary counter xp = 0
C2
Left boundary point xp1 = xpt [xp ++]
C3
Right boundary point xpr = xpt [xp ++]
C4
addr = calculation of the top address of the data in xp1, xpr
C5
C6
L = even number
N
Y
C7
C8
Transfer the data of xpr-xp1 to xp1 of the line memory 16a from addr
Transfer the data of xpr-xp1 to xp1 of the line memory 16b from addr
xp1 = xpr
C9
C10
N
xp >= xpm
Y

FIG. 12A

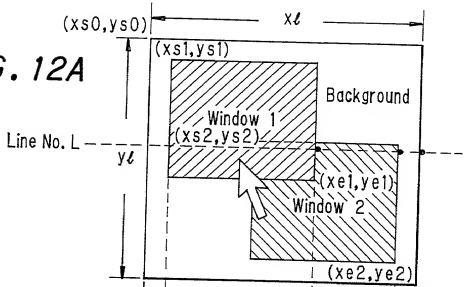


FIG. 12B

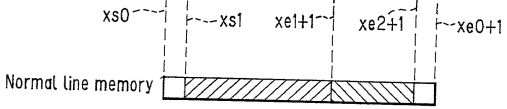


FIG. 13

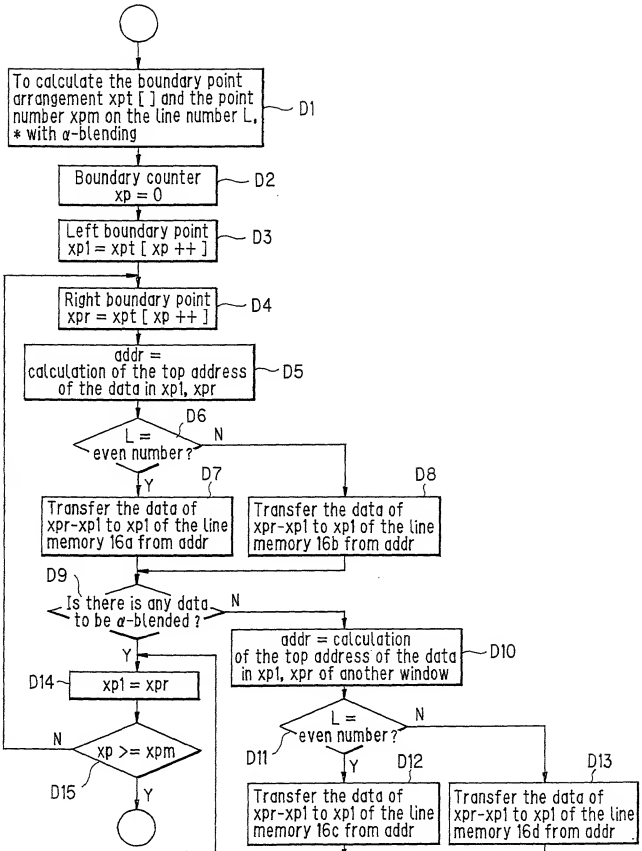

To calculate the boundary point arrangement xpt [ ] and the point number xpm on the line number L, * with α-blending
D1
Boundary counter xp = 0
D2
Left boundary point xp1 = xpt [xp ++]
D3
Right boundary point xpr = xpt [xp ++]
D4
addr = calculation of the top address of the data in xp1, xpr
D5
L = even number?
D6
N
Y
D7
D8
Transfer the data of xpr-xp1 to xp1 of the line memory 16a from addr
Transfer the data of xpr-xp1 to xp1 of the line memory 16b from addr
D9
Is there is any data to be α-blended?
N
Y
addr = calculation of the top address of the data in xp1, xpr of another window
D10
D14
xp1 = xpr
L = even number?
N
Y
D11
D12
D13
N
xp >= xpm
D15
Y
Transfer the data of xpr-xp1 to xp1 of the line memory 16c from addr
Transfer the data of xpr-xp1 to xp1 of the line memory 16d from addr

FIG. 14A

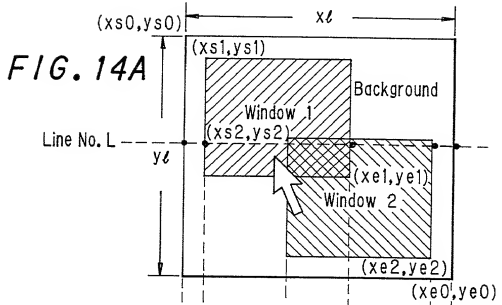


FIG. 14B

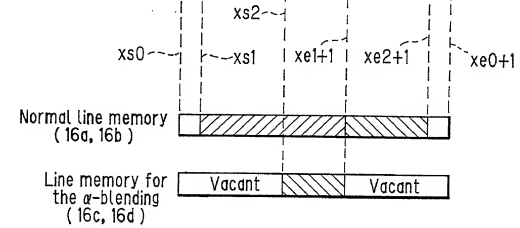


FIG. 15

Control data	State of motionr	Motion of each counter after processing		Write motion
		Readout counter	Write counter	
0 0	normal	+ 1	+ 1	to be done
0 1	contraction	+ 1	+ 0	not to be done
1 0	expansion	+ 0	+ 1	to be done
1 1	skip	+ 0	+ 1	not to be done

FIG. 16

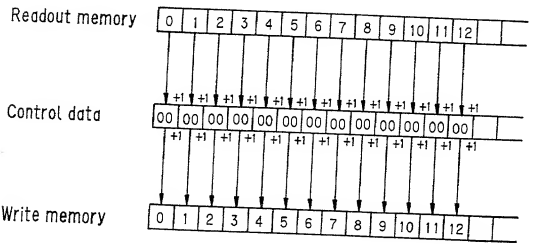


FIG. 17

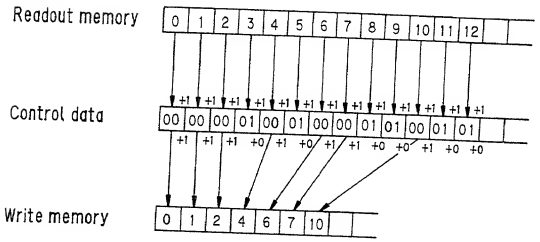

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
00 00 00 01 00 01 00 00 01 01 00 01 01
+1 +1 +1 +0 +1 +0 +1 +1 +0 +0 +1 +0 +0
Write memory
0 1 2 4 6 7 10

FIG. 18

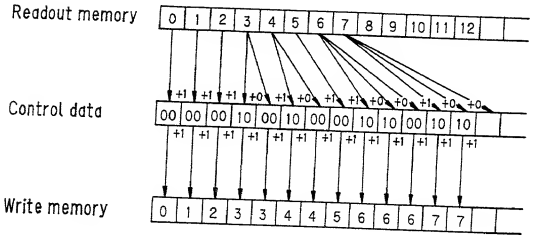

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
00 00 00 10 00 10 00 00 10 10 00 10 10
Write memory
0 1 2 3 3 4 4 5 6 6 6 7 7

FIG. 19

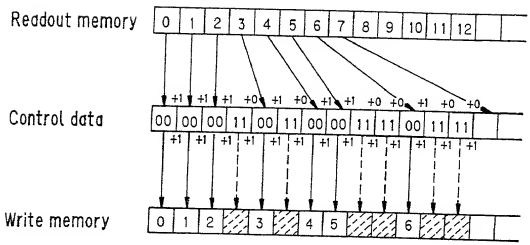

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
00 00 00 11 00 11 00 00 11 11 00 11 11
Write memory
0 1 2 3 4 5 6

FIG. 20

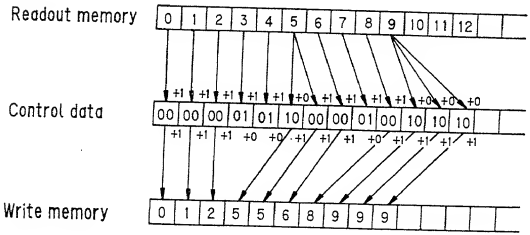

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
00 00 00 01 01 10 00 00 01 00 10 10 10
Write memory
0 1 2 5 5 6 8 9 9 9

FIG. 21

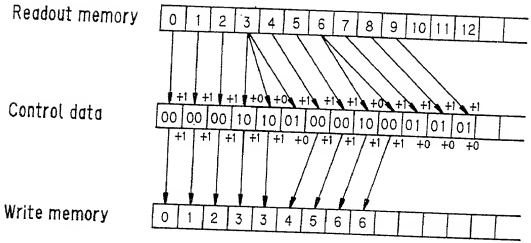

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
00 00 00 10 10 01 00 00 00 10 00 01 01 01
Write memory
0 1 2 3 3 4 5 6 6

FIG. 22

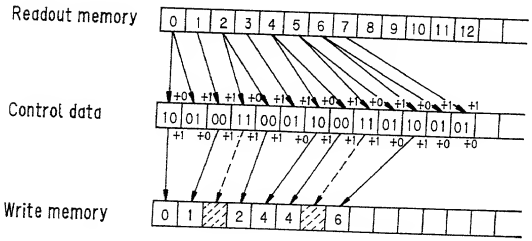

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
10 01 00 11 00 01 10 00 11 01 10 01 01
Write memory
0 1 2 4 4 6

FIG.23

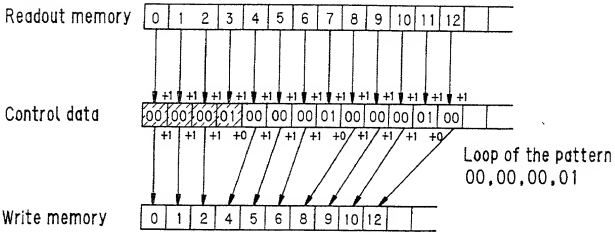

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
00 00 00 01 00 00 00 01 00 00 00 01 00
+1 +1 +1 +0 +1 +1 +1 +0 +1 +1 +1 +0
Loop of the pattern
00,00,00,01
Write memory
0 1 2 4 5 6 8 9 10 12

FIG.24

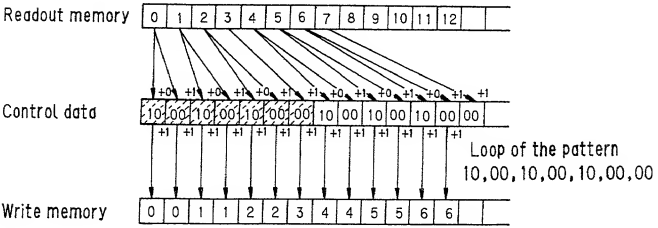

Readout memory
0 1 2 3 4 5 6 7 8 9 10 11 12
Control data
10 00 10 00 10 00 10 00 10 00 10 00 00
+0 +1 +0 +1 +0 +1 +1 +0 +1 +0 +1 +0 +1 +1
Loop of the pattern
10,00,10,00,10,00,00
Write memory
0 0 1 1 2 2 3 4 4 5 5 6 6

FIG. 25

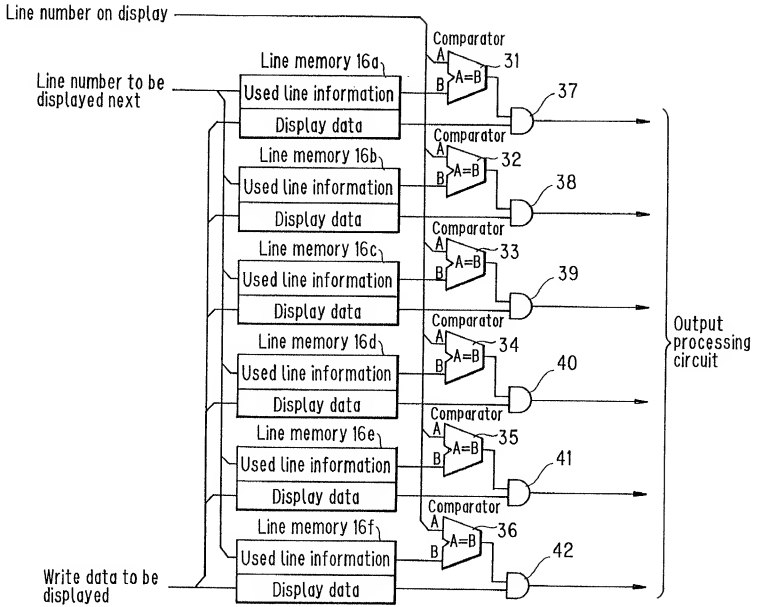


FIG.26A

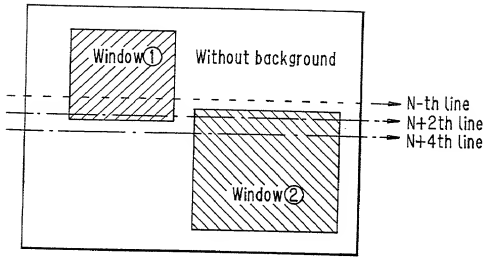


FIG.26B

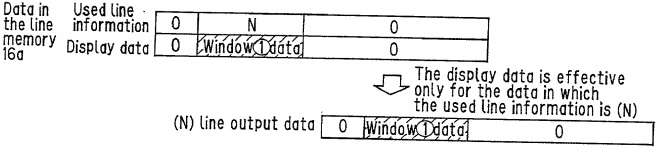


FIG.26C

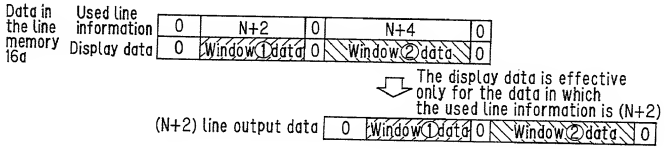


FIG.26D

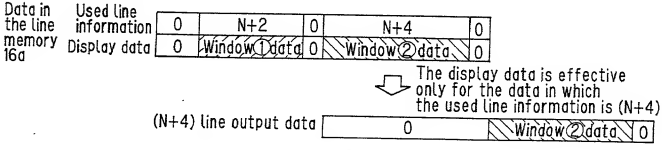
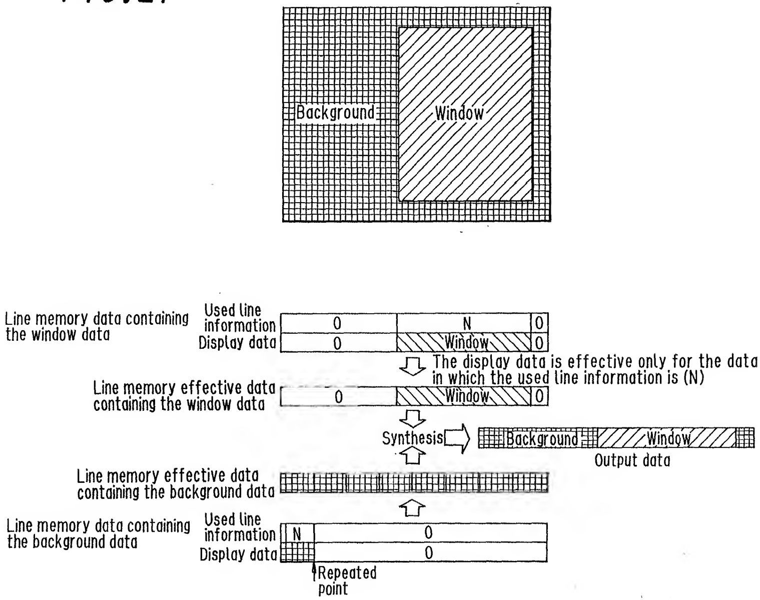


FIG. 27


Background
Window
Line memory data containing the window data
Used line information
Display data
0
N
0
0
Window
0
The display data is effective only for the data in which the used line information is (N)
Line memory effective data containing the window data
0
Window
0
Synthesis
Background
Window
Output data
Line memory effective data containing the background data
Line memory data containing the background data
Used line information
Display data
N
0
0
Repeated point

BIRCH, STEWART, KOLASCH & BIRCH, LLP

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

COMBINED DECLARATION AND POWER OF ATTORNEY

FOR PATENT AND DESIGN APPLICATIONS

ATTORNEY DOCKET NO. 1152-237P

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title: PROGRAMMABLE DISPLAY DEVICE

Fill in Appropriate Information - For Use Without Specification Attached:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as
United States Application Number _____; and /or

the specification was filed on _____ as PCT
International Application Number _____; and was
amended under PCT Article 19 on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority Information: (if appropriate)

Prior Foreign Application(s) (Number)	(Country)	(Month/Day/Year Filed)	Priority Claimed
Hei 9-10592	Patent Japan	Jan./23/1997	☒ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No
			☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

Insert Provisional Application(s): (if any)

(Application Number) (Filing Date)

(Application Number) (Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months (6 Months for Designs) Prior To The Filing Date of This Application:

Insert Requested Information: (if appropriate)

Country	Application No.	Date of Filing (Month/Day/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Insert Prior U.S. Application(s): (if any)

(Application Number) (Filing Date) (Status - patented, pending, abandoned)

(Application Number) (Filing Date) (Status - patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute this application and/or an international application based on this application and to transact all business in the Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the attorneys identified below, unless the inventor(s) or assignee provides said attorneys with a written notice to the contrary:

Terrell C. Birch	(Reg. No. 19,382)	Raymond C. Stewart	(Reg. No. 21,066)
Joseph A. Kolasch	(Reg. No. 22,463)	James M. Slattery	(Reg. No. 28,380)
Bernard L. Sweeney	(Reg. No. 24,448)	Michael K. Mutter	(Reg. No. 29,680)
Charles Gorenstein	(Reg. No. 29,271)	Gerald M. Murphy, Jr.	(Reg. No. 28,977)
Leonard R. Svensson	(Reg. No. 30,330)	Terry L. Clark	(Reg. No. 32,644)
Andrew D. Meikle	(Reg. No. 32,868)	Marc S. Weiner	(Reg. No. 32,181)
Joe McKinney Muncy	(Reg. No. 32,334)	Andrew F. Reish	(Reg. No. 33,443)
C. Joseph Faraci	(Reg. No. 32,350)	Donald J. Daley	(Reg. No. 34,313)

Send Correspondence to: **BIRCH, STEWART, KOLASCH & BIRCH, LLP**

P.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

PLEASE NOTE: YOU MUST COMPLETE THE FOLLOWING:

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of First or Sole Inventor:
Insert Name of Inventor
Insert Date This Document is Signed
Insert Residence
Insert Citizenship
Insert Post Office Address

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Satoshi	NAKAMURA	Satoshi Nakamura	June 25, 1999
Residence (City, State & Country)		CITIZENSHIP	
Sakura-shi, Chiba, Japan	JPX	Japan	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
193-2-C-105, Mutsuzaki, Sakura-shi, Chiba, Japan			

Full Name of Second Inventor, if any: see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Hiroyuki	YAMAMURA	Hiroyuki Yamamura	June 25, 1999
Residence (City, State & Country)		CITIZENSHIP	
Chiba-shi, Chiba, Japan	JPX	Japan	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			
706-2-F201, Kamatori-cho, Midori-ku, Chiba-shi, Chiba, Japan			

Full Name of Third Inventor, if any see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Shinzi	YAMAMOTO	Shinzi Yamamoto	June 25, 1999
Residence (City, State & Country)		CITIZENSHIP	
Chiba-shi, Chiba, Japan	JPX	Japan	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		24-7-A108,	
Honda-cho 2-chome, Midori-ku, Chiba-shi, Chiba, Japan			

Full Name of Fourth Inventor, if any see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Masaaki	MORIYA	Masaaki Moriya	June 25, 1999
Residence (City, State & Country)		CITIZENSHIP	
Chiba-shi, Chiba, Japan	JPX	Japan	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		24-7-A107,	
Honda-cho 2-chome, Midori-ku, Chiba-shi, Chiba, Japan			

Full Name of Fifth Inventor, if any see above

GIVEN NAME	FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP	
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)			

* DATE OF SIGNATURE

(USPTO Approved 8-90)
(Revised 8-97)